

On the origin of the premature breakdown of thermal oxide on 3C-SiC probed by electrical scanning probe microscopy

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Abstract. The dielectric breakdown (BD) of thermal oxide (SiO₂) grown on cubic silicon carbide (3C-SiC) was investigated comparing the electrical behavior of macroscopic metal-oxide-semiconductor (MOS) capacitors with nanoscale current and capacitance mapping using conductive atomic force (C-AFM) and scanning capacitance microscopy (SCM). Spatially resolved statistics of the oxide BD events by C-AFM revealed that the extrinsic premature BD is correlated to the presence of peculiar extended defects, the anti-phase boundaries (APBs), in the 3C-SiC layer. SCM analyses showed a larger carrier density at the stacking faults (SFs) the 3C-SiC, that can be explained by a locally enhanced density of states in the conduction band. On the other hand, a local increase of minority carriers concentration was deduced for APBs, indicating that they behave as conducting defects having also the possibility to trap positive charges. The results were explained with the local electric field enhancement in correspondence of positively charged defects.

Introduction

Thanks to its unique physical and electronic properties, silicon carbide (SiC) is an excellent material for high power and high temperature electronics [1]. Among the different polytypes of SiC, the most mature is the hexagonal 4H-SiC, which is currently available on large area (commercially up to 150 mm, 200mm for R&D substrates) and suitable for the fabrication of power electronics devices. On the other hand, the cubic polytype (3C-SiC) has been studied since a long time, as it could give some advantages with respect to 4H-SiC in metal oxide semiconductor field effect (MOSFET) devices. In fact, due to its smaller band gap, the SiO₂/3C-SiC interface states density at energies close to the conduction band edge is expected to be much lower than that typically measured for SiO₂/4H-SiC interfaces [2,3,4]. Consequently, a high inversion channel mobility is expected in 3C-SiC MOS-based devices. As a matter of fact, in the last decade 3C-SiC MOSFETs with excellent mobility values (50-260 cm²V⁻¹s⁻¹) have been demonstrated in literature [5,6,7,8]. Hence, 3C-SiC is considered a good candidate for power electronics applications in the voltage range 600-900V.

Another potential advantage of the cubic polytype is the possibility to be hetero-epitaxially grown on large diameter cheap silicon (Si) substrates. However, the large lattice mismatch results in 3C-SiC layers with a high density of defects and a notable surface roughness [9]. Hence, both the oxidation process and the final quality of the SiO₂/3C-SiC interfaces will be strongly dependent on the 3C-SiC material [10,11,12,13].

In literature, thermally grown and deposited oxides have been investigated on 3C-SiC [14,15,16]. In both cases, the SiO₂/3C-SiC system often suffers of a premature dielectric breakdown, and is characterized by a high interface state density and large negative shift of the flat band voltage (V_{FB}) [17], indicating the presence of a net positive effective charge in the system. Recently, *Li et al.* [18] observed that the dielectric breakdown kinetics of MOS capacitors is influenced by the gate area and they proposed the existence of at least three different extrinsic and intrinsic breakdown mechanisms responsible for the MOS degradation. However, the origin of each extrinsic mechanism and its relation with the crystalline defects are still unclear.

Clearly, due to the aforementioned issues, MOS-based devices on 3C-SiC materials are still far from a practical application in power electronics.

In this work, the mechanisms that induce a premature breakdown of thermally grown SiO₂ on hetero-epitaxial 3C-SiC/Si layers were investigated by means of both measurement on MOS capacitors and nanoscale electrical characterizations. The origin of the different premature dielectric breakdown behavior was pursued at the nanoscale by conductive atomic force microscopy (C-AFM) and scanning capacitance microscopy (SCM). Particular attention was put on the impact of the 3C-

SiC crystalline defects, like stacking faults (SFs) and anti-phase boundaries (APBs), as they are also known to affect the electrical behavior of Schottky contacts on 3C-SiC [19,20].

Experimental section

For this investigation a 10.2 μm thick 3C-SiC layer has been grown on on-axis Si(100) substrates by chemical vapour deposition (CVD) using silane (SiH_4) and propane (C_3H_8) as silicon and carbon precursors, respectively [21].

The morphology of the oxidized 3C-SiC surface was investigated using a PSIA XE-150 AFM operating in non-contact mode with highly doped silicon tips.

On the oxidised material, lateral capacitors were fabricated with the following procedure. After a sacrificial oxidation and oxide removal to clean deeply the 3C-SiC surface, a thermal oxide was grown at 1150°C for one hour in dry O_2 . Lateral metal-oxide-semiconductor (MOS) capacitors were obtained by defining Ni/Au metal electrodes by means of photolithography and lift-off. In particular, the electrodes consisted in a circular inner gate electrode, 50 μm of radius, surrounded by a large area metal large electrode. With this geometry, the capacitance of the cathode is sufficiently high with respect of that of the inner electrode and can be neglected, as they are connected in series. The capacitance-voltage (C-V) and the current-voltage (I-V) characteristics of the MOS capacitors were measured in a CASCADE Microtech probe station, using a Keysight B1505A parameter analyzer.

Nanoscale electrical characterizations, namely Conductive Atomic Force Microscopy (C-AFM) and Scanning Capacitance Microscopy (SCM), have been performed using a DI3100 system by Bruker with a Nanoscope V controller, equipped with the TUNA module in the case of the current measurements using Bruker boron doped diamond tips that provide a tip contact diameter < 100 nm.

Transmission electron microscopy (TEM) images were collected at 200 kV by a JEOL 2010F microscope equipped with the Gatan imaging filter.

Results and discussion

The material characterization started with the evaluation of surface morphology and the identification of the electrical active defects in the as-grown 3C-SiC before thermal oxidation. In particular, C-AFM was employed to probe the 3C-SiC bare surface conduction as schematically illustrated in Figure 1a. In such configuration, the C-AFM probe slides on the 3C-SiC surface acting as a nano-Schottky contact biased in forward polarization with respect to the silicon substrate working as a large back-contact. Figure 1b and 1c show the surface morphology and the current map, respectively, collected simultaneously with a tip bias of $V_{\text{tip}} = + 0.5\text{V}$. Under this polarization, the

current map (Figure 1c) shows the presence (in an appropriate current range from 0 to 20 pA) of preferential conductive paths with a current level at least one order of magnitude higher than the surrounding 3C-SiC bare material. This observation is consistent with the one reported in a recent C-AFM study of 3C-SiC on silicon, where the nature of the extended conductive defects was elucidated by cross-comparison with atomic resolution structural analyses and ab-initio simulations [20]. In particular, the boundaries between two Anti-Phase 3C-SiC domains were identified by dotted curved lines in Figures 1b and c, and are commonly named Anti-Phase Boundaries (APBs). These are extended defects separating 3C-SiC regions with inverted crystal symmetry, that is, upside-down flipping of the Si-C bond. The APBs appear as curved and randomly oriented features in the C-AFM map. On the other hand, the conductive features appearing as straight lines in Figure 1c were identified as some stacking faults (SFs). These are typical planar crystallographic defects lying on {111} planes of the 3C-SiC polytype, which are terminated as lines with mutually perpendicular orientations on the (100) growth plane.

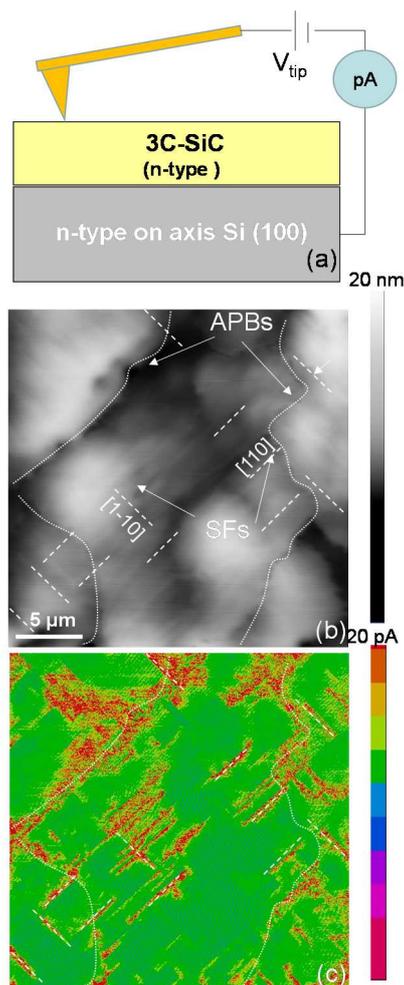


Figure 1: a) Schematic illustration of the setup for the electrical characterization of the 3C-SiC surface by C-AFM. b) Morphology and c) current map collected under forward bias (+0.5 V) of the tip. Both SFs and APBs are visible and more conductive than the surrounding 3C-SiC material.

Figure 2a shows an AFM image of the 3C-SiC material after the thermal growth of SiO₂. The morphology of the as-grown oxide resembles that of the 3C-SiC material, i.e., characterized by *terraces* separated by darker lines associated with the APBs. The SiO₂ surface roughness, evaluated in terms of the root mean square of the heights distribution (RMS), was in the order of 5 nm. This value is comparable to those measured directly on 3C-SiC layer before oxidation, demonstrating the conformal growth of the oxide onto the substrate. Figures 2b and c show two representative cross sectional TEM micrographs collected on the regions where a SF (b) and an APB (b) reach the 3C-SiC/SiO₂ interface. A conformal oxide growth, without any thickness variations at defects positions, can be clearly observed.

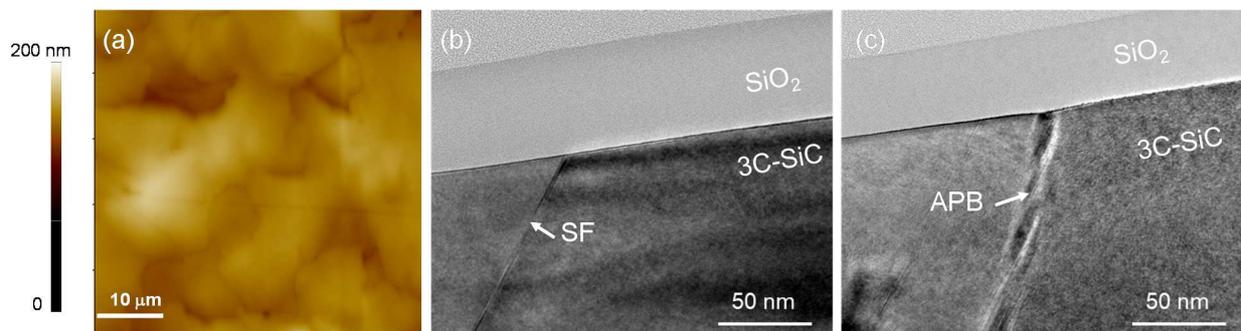


Figure 2. AFM morphology image of the thermal SiO₂ grown on 3C-SiC (a) and cross-sectional TEM micrographs in the SF region (b) and in the APB region (c) respectively. No thickness variation of the SiO₂ layer can be observed.

On this material, lateral MOS capacitors were fabricated according to the schematic shown in Figure 3a. Figure 3b shows the optical microscope image of the top of the MOS capacitors with the indication of the gate (anode) area separated by the cathode.

Firstly, the electrical quality of the oxide was evaluated by means of capacitance - voltage (C-V) and current density - voltage (J-V) measurements on MOS capacitors. Figure 3c shows the experimental C-V curve compared with the theoretical one. From the value of the depletion capacitance, the net doping concentration of the 3C-SiC layer was estimated to be $N_D = 2 \times 10^{16} \text{ cm}^{-3}$.

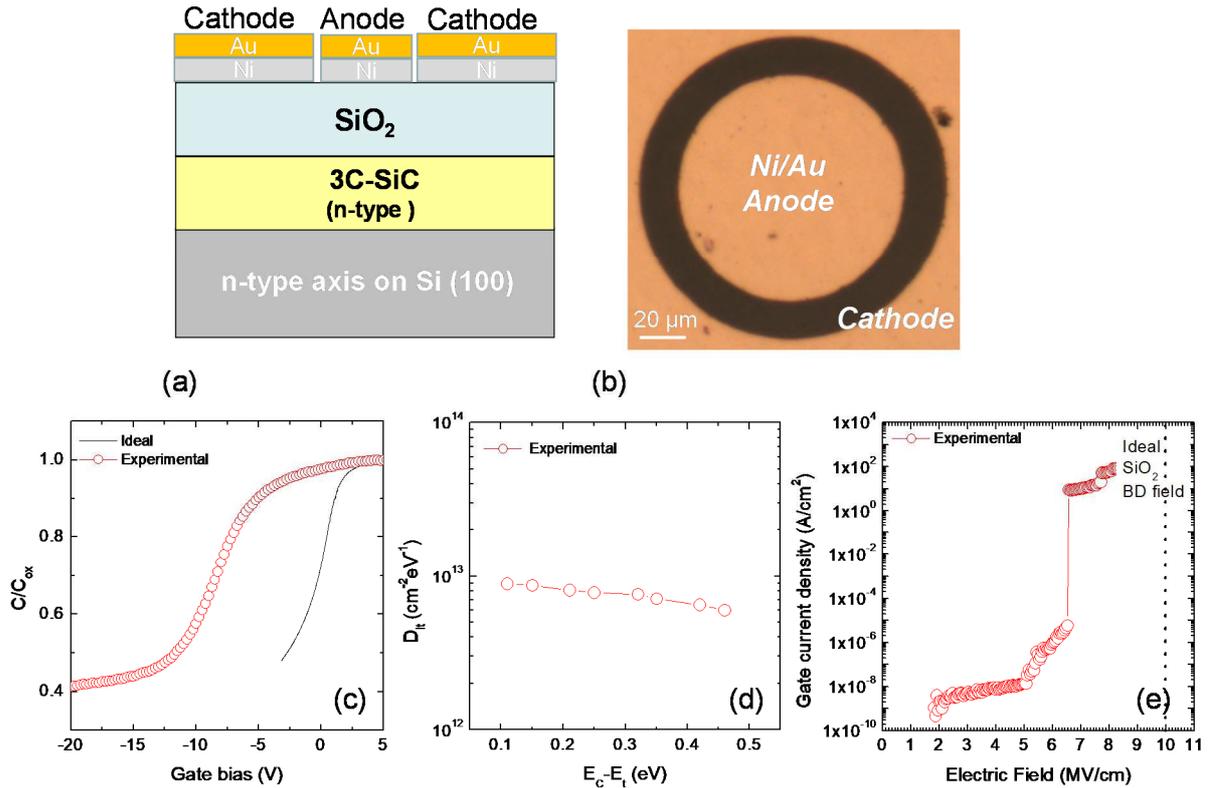


Figure 3: (a) Schematic in cross-section of the lateral MOS capacitor fabricated on thermally oxidized 3C-SiC; (b) optical microscope image of a MOS capacitor; (c) Experimental C-V curve measured on 3C-SiC MOS capacitors compared with the theoretical curve; (d) Experimental interface state density energetic distribution; (e) Current density vs voltage (J-V) curve measured on 3C-SiC MOS capacitors. The value of the ideal SiO₂ breakdown electric field is indicated by the dashed line.

The oxide thickness, estimated from the accumulation capacitance (C_{ox}), is about 40 nm. The experimental C-V curve is negatively shifted with respect to the ideal C-V curve and has a flat band voltage (V_{FB}) of about -7.5 V (Figure 3c). The observed V_{FB} negative shift (Fig. 3a) corresponds to an amount of positive effective charge in the MOS system of $N_{eff} = +3 \times 10^{12} \text{ cm}^{-2}$. A similar negative flat band voltage shift has been observed by *Sharma et al.* [15] on thermal oxides on 3C-SiC grown in the 1200-1400°C range. In particular, they showed that the V_{FB} shift increased with increasing the oxidation temperature [15]. The origin of the positive effective charge is still debated, and has been attributed to the presence of carbon clusters, positively or negatively charged O-H-C-Si complexes, and dangling bonds formed after thermal oxidation [22].

The interface states density (D_{it}) energy profiles below the 3C-SiC conduction band edge, estimated using the conductance method, are depicted in Fig. 3d. The maximum value, measured at 0.1 eV below the conduction band, was $8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. These D_{it} values are in the same order of magnitude of the typical values reported for thermal oxides on 3C-SiC [15,16].

Finally, Fig. 3e shows the J-V curve collected on the lateral MOS capacitor. As can be seen, the breakdown field is significantly lower with respect to the theoretical value for SiO₂ (~10 MV/cm) [23]. In fact, the experimental BD field is about 6.5 MV/cm.

To get a deeper insight on the origin of this discrepancy, a nanoscale electrical characterization of the SiO₂/3C-SiC system will be presented in the remaining part of this paper.

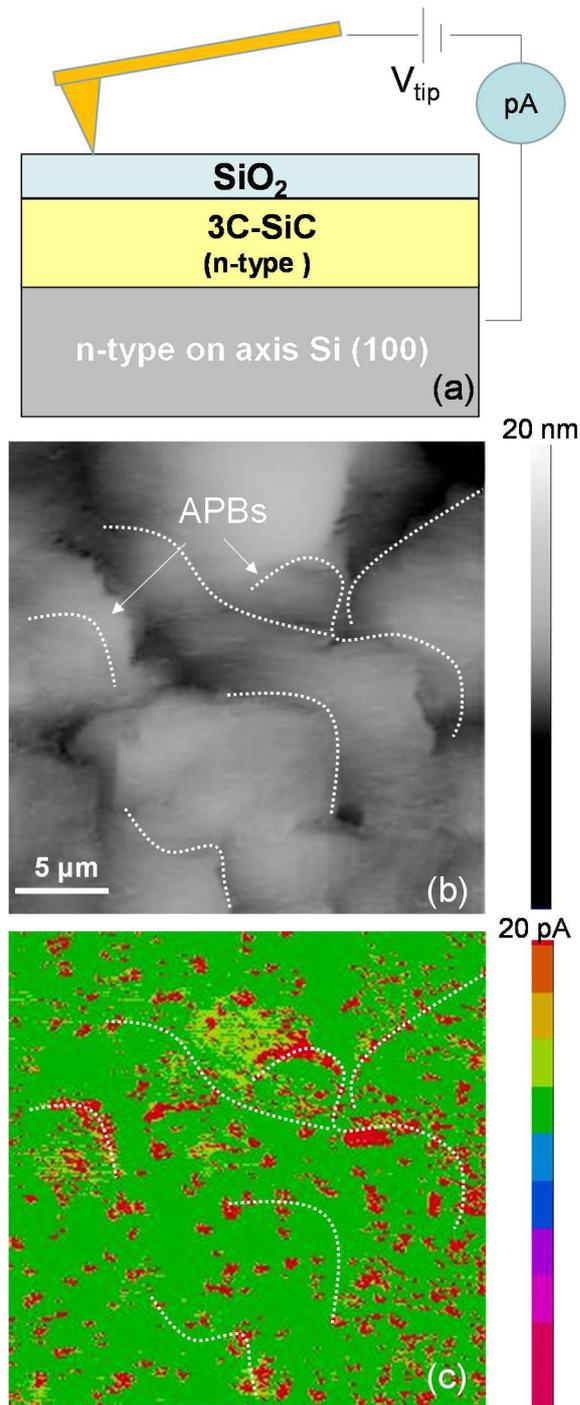


Figure 4: a) Schematic illustration of the setup for the electrical characterization of the SiO₂/3C-SiC system by C-AFM. b) Morphology and c) current map collected under high electric field (8 MV/cm) of the tip.

Nanoscale resolution current mapping by C-AFM [24,25,26] is a powerful method to investigate the role played by defects on the dielectric breakdown behavior of thin insulators [27]. In order to explain the origin of the premature breakdown observed at the macroscopic level in MOS capacitors, thin thermal oxides (~ 10 nm) were characterized at a nanoscale level by means of C-AFM stress measurements at very high electric field (> 8 MV/cm), i.e., close to the ideal breakdown field value of silicon dioxide (~10 MV/cm) and above the experimental breakdown field (~6.5 MV/cm) measured on macroscopic SiO₂/3C-SiC capacitors (Figure 3e). Figure 4a shows a schematic illustration of the experimental setup used for nanoscale C-AFM analyses of the SiO₂/3C-SiC system. Figures 4b and 4c report simultaneously collected AFM morphology and current map by the positively bias conductive diamond tip with $V_{\text{tip}}=8$ V. The C-AFM current map in Fig. 4c can be considered as a breakdown map of an array of nano-MOS capacitors (with areas corresponding to the tip contact area) simultaneously stressed at 8 MV/cm for each nano-device. Then, the position of the BD spots in red in Figure 4c have been correlated with the surface morphology (Figure 4b). As can be seen, the BD events are not randomly distributed but there are some regions with a larger density compared with the surroundings. Drawing a dashed line to guide the eye it is possible to see the correspondence on the morphology (Figure 4b) of weak lines located in correspondence with some APBs, already identified in the current maps of the bare 3C-SiC surface (Figure 1c). Noteworthy, the straight lines conductive features associated to SF in the bare 3C-SiC surface were not visible in the case of 3C-SiC covered by thermal SiO₂. It can be also noticed that the edges of the 3C-SiC crystalline terraces seem to have no influence on the nano-MOS premature breakdown.

C-AFM maps allowed to identify the weak points responsible of premature breakdown. In addition, accelerated stress tests of the thin SiO₂ layer could be performed at the nanoscale, by varying the stress time applied by the tip according to the experimental procedure illustrated in Refs. [28,29]. More specifically, the stress time for each nano-MOS was varied by changing the scan rate of the tip (i.e., the scan time per line T that can be varied from 1 s up to 10 min) and the image scan size (i.e., the scan line length L that can be varied from 200 nm up to 100 μm). In this way the stress time applied by the biased conductive diamond tip, expressed as $t_{\text{stress}}= T/(L/a)$ with $a\approx 100$ nm the tip diameter, was varied over about 3 orders of magnitude. The amount of nano-MOS that survived to a given stress time was evaluated from the current maps acquired at the different stress times. Hence, such a variable time stress measurements enabled to count the cumulative failure rate according to the Weibull statistics [30].

As an example, a comparison between two sequential current maps collected in the same position (namely the same array of nano-MOS) is shown in Figure 5. In particular, Figures 5a and 5b show the current maps collected by the C-AFM stressing each nano-MOS at fixed bias for 2s and 50s, respectively. Figure 5c shows the comparison between the distribution of the current flowing through

all the nano-MOS after stress time of 2s and 50s, respectively. As can be noticed, for the 2s stress time, the current values distribution (at 8 MV/cm) is mainly centered at the bottom of the sensitivity of the C-AFM (100 fA) and only few nano-MOS capacitors show current values in the 12 pA range. On the other hand, for the 50s stress time, the current values distribution (at 8 MV/cm) is bimodal with a peak at 100 fA and a sharp peak at current larger than 12 pA (the upper sensitivity value of the C-AFM). Hence, in the same map there are nano-MOS where the current value is suddenly increased up to three orders of magnitude, which can be identified as the breakdown events.

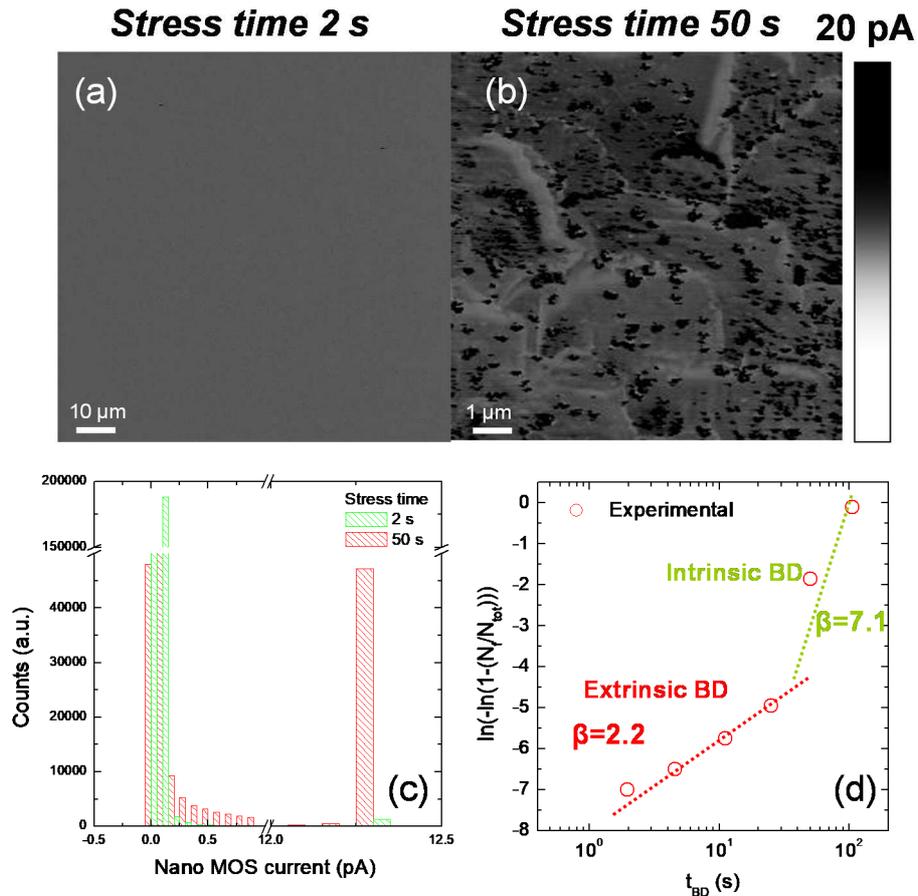


Figure 5: C-AFM current maps acquired under high electric field (8 MV/cm) of the tip with a stress time of 2s (a) and 50s (b); (c) Distributions of the current values flowing in the nano-MOS after stress times of 2s and 50s; (d) Breakdown kinetics and Weibull plots. The intrinsic and extrinsic BD mechanisms are highlighted by dashed lines.

Fig. 5d shows the Weibull's plot obtained after stressing the total amount (N_{tot}) of nano-MOS array for different times. As described in Fig. 4, the number (N) of failed nano-MOS increases increasing the stress time. At low values of the stress time, the Weibull plot has a low slope $\beta = 2.2$. This value is smaller than expected for a 10 nm thick insulator layer [31]. This result demonstrates the presence of an extrinsic breakdown mechanism that induces the premature failure of the nano-MOS. However, as already seen in other works [12,24], at high stress time it is possible to identify the regions of the insulator having a nearly ideal breakdown mechanism with a Weibull slope $\beta = 7.1$ (Fig. 5d). This behavior is in agreement with the prediction of the percolation theory [32] for a 10 nm thick SiO_2 layer.

The combination between the experimental results presented in Figures 1, 4 and 5 suggest that both SFs and APBs are conductive extended defects in the 3C-SiC material, but only APBs are the responsible of the premature BD of the SiO₂/3C-SiC nano-MOS structures. In fact, the breakdown events could be not correlated to the geometry of the SFs (Figure 1c).

Using C-AFM local stress measurements, *Kozono et al.* [33] correlated the BD events at SiO₂/4H-SiC interfaces with the step-bunching edges on the semiconductor surface, attributing the premature BD to the local electric field crowding on these morphological features.

Our results shown in Figure 2 and in Figure 4 suggest that the 3C-SiC morphological features have only a marginal impact on the BD kinetics of the nano-MOS. On the other hand, the impact of the APBs is prominent on the BD kinetics. Hence, the origin of the premature BD in correspondence of the APBs has to be pursued in the electronic nature of the defect and its impact on the MOS system.

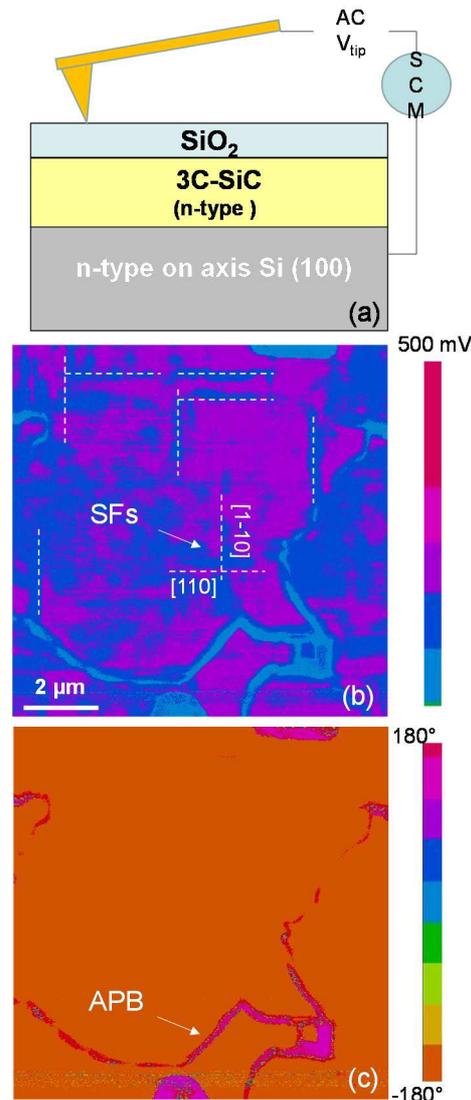


Figure 6: (a) Schematic illustration of the setup for the electrical characterization of the SiO₂/3C-SiC system by SCM; (b) SCM amplitude and (c) SCM phase collected under low signal (< 2 V_{AC}) of the tip.

In order to further elucidate the role of the extended defects in 3C-SiC on the electrical behaviour of the SiO₂/3C-SiC MOS capacitor, capacitance measurements were performed also at nanoscale [34] using the SCM technique. A schematic representation of the SCM experimental setup is illustrated in Figure 6a. During the SiO₂ surface scan with the diamond tip, an AC modulating bias at 100 kHz frequency and with amplitude $\Delta V=2V$ (below the conduction regime through the insulator) was applied to the sample, and the capacitance variation ΔC in response to this modulation was recorded with the SCM sensor. Figure 6b and 6c show two representative images of the SCM signal amplitude $|\Delta C|$ and of the phase signal. In particular, both straight line features resembling SFs (dashed lines) and curved line features resembling APBs can be distinguished in the SCM amplitude image in Figure 6b, whereas only APBs features can be observed in the phase map in Figure 6c. Lateral variations of the SCM signal amplitude in a nanoMOS capacitors can be related to local changes in the insulator thickness/permittivity or in the semiconductor depletion region underneath the tip (related to the local carrier density) [35]. However, since a uniform and conformal SiO₂ layer was shown by cross-sectional TEM analyses for the SiO₂/3C-SiC system under investigation (see Figures 2b and 2c), it can be concluded that the spatial variations in the SCM amplitude are related to local changes in the carrier density in the 3C-SiC layer. In particular, the lower $|\Delta C|$ values measured in Figure 6b on SFs as compared to the surrounding material suggests a locally higher carrier density.

Although the donor concentration incorporated in the 3C-SiC layer during the growth is expected to be uniform, the presence of defects (such as SFs and APBs) is known to be responsible of modifications of the 3C-SiC electronic band-structure with respect to defects' free regions [20], ultimately resulting in a change of the local carrier density in the 3C-SiC material. In particular, in the presence of a SF a significant enhancement of the density of states (DOS) both in the valence and the conduction band of 3C-SiC has been predicted by ab-initio calculations [20]. This can explain both the enhanced SFs conductivity observed in the C-AFM maps on the bare 3C-SiC surface (see Figure 1c) and the larger electron density deduced from the SCM amplitude map (see Figure 6b). Hence, SFs can be considered as highly conducting 2D defects.

Interestingly, Figure 6c shows a strong change of the SCM phase signal from 180° on APBs to -180° on the surrounding regions. The phase signal is known to be very sensitive to the type of majority carriers in the semiconductor. In the present case, the variation of the SCM phase can be also indicative of a local increase of the minority carriers (holes) concentration in the 3C-SiC material. Similar results have been recently obtained by SCM phase analyses performed on threading dislocations of 4H-SiC [36], which served to demonstrate an increase of minority carriers concentration in the volume surrounding these killer defects responsible of BD of 4H-SiC power MOSFETs after prolonged stress [36]. In the specific case of 3C-SiC, ab-initio calculations indicated that a peculiar property of APBs is that these defects introduce states within the 3C-SiC bandgap

close to the valence band [20]. Thus, the APBs may act also as a preferential sites for positive charges trapping. The presence of positively charged defects at the SiO₂/3C-SiC interface is also in agreement with the negative flat band shift observed in the macroscopic MOS structures (Figure 2c).

In this scenario, an impact of the APBs in the accelerated BD kinetics can be argued. In fact, the accelerated BD occurred when a positive electric field is applied to the nano-MOS. Figure 7a shows the band gap diagram under the application of an electric field to the ideal nano-MOS. For a given potential applied to the gate (V_{tip}) the actual electric field value depends on the insulator thickness (t_{ox}), on the flat-band voltage (V_{FB}) and on the amount of effective positive charge (N_{eff}) in the nano-MOS:

$$E_{ox} = \frac{V_{tip} - V_{FB}}{t_{ox}} + q \frac{N_{eff}}{t_{ox}}$$

where q is the elementary electron charge.

Clearly, for a given V_{tip} on the gate of the nano-MOS, the electric field is minimum in the ideal case (Figure 7a), while it is increased in the presence of positive charge trapping in the APBs (Figure 7b). The local increase of the electric field in correspondence of the APBs produces the increase of the local current flow related to the increase of the injected electrons from the 3C-SiC substrate into the insulating layer. Hence, the increased local electron injection accelerate the dielectric breakdown, producing extrinsic breakdown events. A similar role of charged interfacial defects has been invoked by *Arvanitopoulos et al.* [37] to describe the anomalous experimental current behaviour through Schottky barriers on 3C-SiC. Accordingly, the charged defects at the metal/3C-SiC interface induce an electrostatic thinning of the Schottky barrier, resulting in an enhanced current conduction.

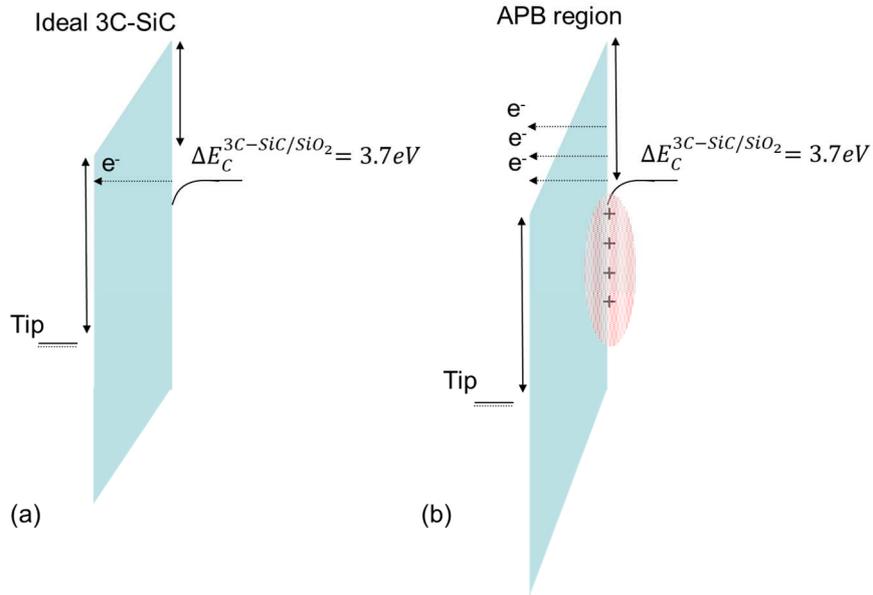


Figure 7: Schematic band diagram of the SiO₂/3C-SiC nano-MOS, when a high tip bias is applied (a) in the ideal material and (b) in the APB region. The positive charge trapped in the APB produces an increase of the electric field that enhances the tunnelling current from electrons injected from the substrate into the insulator accelerating its degradation.

Conclusion

In this paper, the origin of the premature breakdown behavior of thermal oxide grown on 3C-SiC/Si hetero epitaxial layers has been investigated, employing electrical scanning probe microscopy techniques and standard characterization on large area MOS capacitors. In particular, the nanoscale Weibull statistic plot obtained by C-AFM on the nano-MOS revealed a non-negligible population of extrinsic breakdown events. Those extrinsic BD events are correlated to the presence of anti-phase boundaries (APBs) in the 3C-SiC. SCM characterization on the oxide allowed to demonstrate that the stacking faults (SFs) possess a larger density of states in the 3C-SiC conduction band. On the other hand, the SCM phase signal in proximity of the APBs was interpreted with the presence of positive trapped charge. Basing on these nanoscale results, the premature dielectric breakdown observed in large area MOS capacitors has been explained interpreted by the presence of positively charged APBs, which cause an enhanced electron injection from the semiconductor into the insulator. This model agrees with the localization of the extrinsic BD in correspondence of the APBs.

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